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CLAIMS

What is claimed is:

1. A memory cell comprising:

an access device formed on a semiconductor substrate;

a layer of dielectric material disposed on said access device, said layer of dielectric material having a pore therein, said pore being smaller than a photolithographic limit;

a first layer of conductive material disposed within said pore to form a first electrode;

a layer of structure changing material disposed on said first electrode; and

a second layer of conductive material disposed on said layer of structure changing material to form a second electrode.

2. The memory cell, as set forth in claim 1, wherein said access device comprises a diode.

3. The memory cell, as set forth in claim 2, wherein said diode comprises:

a layer of N doped polysilicon disposed on said substrate; and

a layer of P+ doped polysilicon disposed on said N doped layer of polysilicon.

4. The memory cell, as set forth in claim 1, wherein said structure changing material comprises a chalcogenide material.

5. The memory cell, as set forth in claim 1, further comprising a layer of insulative material substantially surrounding said access device, said layer of dielectric material, said layer of structure changing material, and said upper electrode.

6. The memory cell, as set forth in claim 1, wherein said layer of structure changing material is disposed in said pore.

7. A memory array comprising:

a plurality of memory cells, each memory cell comprising:

an access device formed on a semiconductor substrate;

a layer of dielectric material disposed on said access device, said layer of dielectric material having a pore therein, said pore being smaller than a photolithographic limit;

a first layer of conductive material disposed within said pore to form a first electrode;

a layer of structure changing material disposed on said first electrode; and

a second layer of conductive material disposed on said layer of structure changing material to form a second electrode; and

a grid coupled to said plurality of memory cells, said grid formed by a first plurality of conductive lines generally extending in a first direction and a second plurality of conductive lines generally extending in a second direction.

8. The memory array, as set forth in claim 7, wherein said access device comprises a diode.

9. The memory array, as set forth in claim 8, wherein said diode comprises:

a layer of N doped polysilicon disposed on said substrate; and

a layer of P+ doped polysilicon disposed on said N doped layer of polysilicon.

10. The memory array, as set forth in claim 7, wherein said structure changing material comprises a chalcogenide material.

11. The memory array, as set forth in claim 7, wherein each of said plurality of memory cells further comprises a layer of insulative material substantially surrounding said access device, said layer of dielectric material, said layer of structure changing material, and said second electrode.

12. The memory array, as set forth in claim 7, wherein said layer of structure changing material is disposed in said pore.

13. The memory array, as set forth in claim 7, wherein said plurality of memory cells are arranged in a plurality of generally perpendicular rows and columns.

14. The memory array, as set forth in claim 13, wherein each of said first plurality of conductive lines are coupled to memory cells in a respective row, and wherein each of said second plurality of conductive lines are coupled to memory cells in a respective column.

15. A method of fabricating a memory cell, said method comprising the steps of:

(a) forming an access device on a semiconductor substrate;

(b) depositing a layer of dielectric material on said access device;

(c) forming a pore in said layer of dielectric material, said pore being smaller than a photolithographic limit;

(d) depositing a first layer of conductive material within said pore to form a first electrode;

(e) depositing a layer of structure changing material on said first electrode, and

(f) depositing a second layer of conductive material on said layer of structure changing material to form a second electrode.

16. The method, as set forth in claim 15, wherein step (a) comprises the step of forming a diode.

17. The method, as set forth in claim 16, wherein the step of forming a diode comprises the steps of:

forming a layer of N doped polysilicon disposed on said substrate; and

forming a layer of P+ doped polysilicon disposed on said N doped layer of polysilicon.

18. The method, as set forth in claim 15, wherein step (c) comprises the steps of:

forming a mask over said layer of dielectric material, said mask having a window therein exposing a portion of said layer of dielectric material, said window being sized at said photolithographic limit;

forming a spacer within said window, said spacer covering a peripheral portion of said exposed portion of said layer of dielectric material to create a second window exposing a portion of said layer of dielectric material smaller than said photolithographic limit; and

removing said exposed portion of said layer of dielectric material created by said second window to create said pore.

19. The method, as set forth in claim 15, wherein step (d) comprises the steps of :

depositing said first layer of conductive material onto said layer of dielectric material and into said pore using collimated physical vapor deposition; and

removing portions of said first layer of conductive material deposited onto said layer of dielectric material.

20. The method, as set forth in claim 15, wherein step (e) comprises the step of :

depositing a layer of chalcogenide material on said first electrode.

21. The method, as set forth in claim 15, wherein step (e) comprises the step of:

depositing said layer of structure changing material in said pore.

22. The method, as set forth in claim 15, further comprising the step of:

forming a layer of insulative material substantially surrounding said access device, said layer of dielectric material, said layer of structure changing material, and said second electrode.

23. A method of fabricating a memory array, said method comprising the steps of:

(a) forming a plurality of access devices on a semiconductor substrate;

(b) forming a first plurality of conductive lines, each of said first plurality of conductive lines being coupled to respective access devices;

(c) depositing a layer of dielectric material on said access devices;

(d) forming a plurality of pores in said layer of dielectric material, each of said pores being smaller than a photolithographic limit;

(e) depositing a first layer of conductive material within each of said pores to form a plurality of first electrodes;

(f) depositing a layer of structure changing material on each of said first electrodes;

(g) depositing a second layer of conductive material on said layer of structure changing material to form a plurality of second electrodes; and

(h) forming a second plurality of conductive lines, each of said second plurality of conductive lines being coupled to respective second electrodes.

24. The method, as set forth in claim 23, wherein step (a) comprises the step of forming a plurality of diodes.

25. The method, as set forth in claim 24, wherein the step of forming said plurality of diodes comprises the steps of:

forming a layer of N doped polysilicon disposed on said substrate; and

forming a layer of P+ doped polysilicon disposed on said N doped layer of polysilicon.

26. The method, as set forth in claim 23, wherein step (d) comprises the steps of:

forming a mask over said layer of dielectric material, said mask having a plurality of windows therein exposing portions of said layer of dielectric material, said windows being sized at said photolithographic limit;

forming a spacer within each of said windows, each spacer covering a peripheral portion of said respective exposed portions of said layer of dielectric material to create a second window exposing a portion of said layer of dielectric material smaller than said photolithographic limit; and

removing said exposed portions of said layer of dielectric material created by said second windows to create said pores.

27. The method, as set forth in claim 23, wherein step (e) comprises the steps of:

depositing said first layer of conductive material onto said layer of dielectric material and into said pores using collimated physical vapor deposition; and

removing portions of said first layer of conductive material deposited onto said layer of dielectric material.

28. The method, as set forth in claim 23, wherein step (f) comprises the step of :

depositing a layer of chalcogenide material on said first electrodes.

29. The method, as set forth in claim 23, wherein step (f) comprises the step of:

depositing said layer of structure changing material in said pores.

30. A method of fabricating an array of pores, said method comprising the steps of:

forming a mask over a layer of dielectric material, said mask having a plurality of windows therein exposing portions of said layer of dielectric material, said windows being sized at said photolithographic limit;

forming a spacer within each of said windows, each spacer covering a peripheral portion of said respective exposed portions of said layer of dielectric material to create a second window exposing a portion of said layer of dielectric material smaller than said photolithographic limit; and

removing said exposed portions of said layer of dielectric material created by said second windows to create said pores.

31. A memory cell comprising:

an access device formed on a semiconductor substrate;

a layer of dielectric material disposed on said access device, said layer of dielectric material having a pore therein, said pore being formed by forming a mask over said layer of dielectric material, said mask having a window therein exposing a portion of said layer of dielectric material, said window being sized at said photolithographic limit, forming a spacer within said window, said spacer covering a peripheral portion of said exposed portion of said layer of dielectric material to create a second window exposing a portion of said layer of dielectric material smaller than said photolithographic limit, and removing said exposed portion of said layer of dielectric material created by said second window to create said pore;

a first layer of conductive material disposed within said pore to form a first electrode;

a layer of structure changing material disposed on said first electrode; and

a second layer of conductive material disposed on said layer of structure changing material to form a second electrode.

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